IN THE DRAWINGS:

Concurrently herewith, there is submitted a Request for Permission to Change the Drawings. Applicant requests approval of the revisions contained therein.

REMARKS

Claims 1-16 are pending. The drawings have been amended. Reconsideration of the application is respectfully requested.

Claims 3, 10, and 15 stand rejected under 35 U.S.C. 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

According to the Examiner, in "claim 3, it is unclear how the recitation 'first pair of transistors', 'current source', 'second pair', and 'third pair' is read on the preferred embodiment. Insofar as understood, no such elements can be determined on the drawings. The same is true for claims 10 and 15."

In response to this rejection, Applicants respectfully assert that each of these elements are shown in the drawings. For example, with reference to Fig. 3a, a first pair of transistors is transistor T1/T2. Here, one example of a current source is $Icont_2$. It follows that upon establishment of this convention, one of ordinary skill in the art can readily proceed through the claims and identify each of the claimed components to determine the scope of the claims. Accordingly, Applicants respectfully assert that the claims are definite, and reconsideration and withdrawal of the rejections are therefore in order.

Claims 1-16 stand rejected under 35 U.S.C.(b) as being anticipated by Fig. 1 of the Applicants' admitted prior art. This rejection is respectfully traversed.

Claim 1 includes the limitation "an active load connected to receive as input the current output of [a] trans-admittance circuit and produce a voltage output."

In the present invention, the passive load resistance 120 in Figure 1 is replaced with an active load resistance, such as a trans-impedance stage to increase the gain of the claimed logic circuit. An active load resistance provides more gain at a higher bandwidth A digital circuit comprising several conventional digital gates as shown in Figure 1 is divided into blocks and regrouped to provide current rather than voltage interfaces at the inputs and outputs (see page 3, lines 18 thru 20 of the specification). However, Fig. 1 of the admitted prior art fails to teach the limitation "an active load connected to receive as input the current output of said trans-admittance circuit and produce a voltage output," as set forth in independent claim 1.

In addition, the circuit shown in Fig. 1 fails to teach that the active load is a trans-impedance stage circuit. In accordance with the present invention, the load resistors in the RL - TAS latch, shown in Figure 2b, is replaced with an active resistance load, for example, a trans-impedance amplifier stage (TIS). Figure 3a is a TAS - TIS latch in which the passive load resistance RL comprising R1, R2 has been replaced with an active TIS load including transistors T9, T10, T11, T12 and resistors R3, R4, R5, R6. The TIS load converts an input current to an output voltage. It follows that the circuit shown in Figure 1 fails to teach that the "active load is a trans-impedance stage circuit, as set forth and claimed in independent claim 7, or "two independent combined trans-admittance and trans-impedance stages," as set forth in independent claim 14.

Logic gates configured in accordance with the present invention are less sensitive to transistor collector capacitance and/or wiring capacitance on the collectors of the transistors T3, T4, T5, T6. In addition, the topology shown in Figure 3a provides a convenient node in the circuit that can be used for input/output connections between logic gates. Specifically, logic gates in accordance with the present invention are arranged to have a TIS input stage and a TAS output stage. Thus, the current from the switched TAS output is received by the TIS input stage of the next logic block in the cascaded logic chain, whereas in the conventional logic circuit shown in provides voltages at the outputs (e.g. V-out and V-outb). This claimed configuration is entirely different than the configuration set forth in Fig. 1 of the specification.

In sum, the circuit shown in Figure 1 fails to teach "an active load connected to receive as input the current output of said trans-admittance circuit and produce a voltage output," as set forth in independent claim 1," or that "an active load is a trans-impedance stage circuit," as set forth and claimed in independent claim 7, or "two independent combined trans-admittance and trans-impedance stages," as set forth in independent claim 14. In view of the foregoing, Applicants respectfully assert that independent claims 1, 7 and 14 are patentable over the prior art circuit disclosed in Figure 1 of Applicants' specification and therefore, reconsideration and withdrawal of the rejections are respectfully requested.

In view of the patentability of independents claims 1, 7, and 14 for the reasons set forth above, dependent claims 2-6, 8-13 and 15-16 are also patentable over the cited references.

In light of the foregoing amendments and remarks, this application should be in condition for allowance. Early passage of this case to issue is respectfully requested. However, if there are any questions regarding this Response, or the application in general, a telephone call

to the undersigned would be appreciated since this would expedite the prosecution of the application for all concerned.

Respectfully Submitted,

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COMPLETE SET OF PENDING CLAIMS

1. A latch comprising:

a clocked trans-admittance stage circuit for receiving a voltage and producing a current output; and

an active load connected to receive as input the current output of said trans-admittance circuit and produce a voltage output.

2. The latch in accordance with claim 1, wherein the active load is a trans-impedance stage circuit.

3. The latch in accordance with claim 1, wherein said trans-admittance stage circuit comprises:

a first pair of transistors including a first transistor and a second transistor, the first and second transistors each having a base, an emitter, and a collector;

a current source connected to the emitter of each of said first and second transistors;

a second pair of transistors including a third transistor and a fourth transistor, each of said third and fourth transistors having a base, an emitter, and a collector; and the emitter of each of said third and fourth transistors being connected to the collector of said first transistor; and

a third pair of transistors including a fifth transistor and a sixth transistor, each of said fifth and sixth transistors having a base, an emitter, and a collector; and

the emitter of each of said fifth and sixth transistors being connected to the collector of said second transistor.

4. The latch in accordance with claim 3, wherein the base of said first and second transmitters being clocked on opposite phases of a clock signal.

5. The latch in accordance with claim 4, wherein the base of said third transistor receives as input a voltage signal and the base of said fourth transistor receives as input an inverted voltage signal, said third transistor produces a current output signal based on the inverted voltage signal, and said fourth transistor produces an inverted current output signal based on the voltage signal.

6. The latch in accordance with claim 1, further comprising transmission lines coupled between said clocked trans-admittance circuit and said active load.

7. A cascaded latch chain comprising:

a clocked trans-admittance stage latch receiving an input voltage and producing an output current.

8. The cascaded latch in accordance with claim 7, further comprising at least one latch pair connected to receive the output current of said clocked trans-admittance stage latch and producing an output current, said at least one latch pair including two independent combined trans-admittance and trans-impedance stages.

9. The cascaded latch chain in accordance with claim 8, comprising at least two latch pairs including a first latch pair and a last latch pair, each latch pair having two independent trans-admittance and trans-impedance stages, the two trans-admittance and trans-impedance stages of each latch pair being clocked on opposite phases of a clock signal.

10. The cascaded latch chain in accordance with claim 9, wherein said trans-admittance stage in each latch pair comprises:

a first pair of transistors including a first transistor and a second transistor, the first and second transistors each having a base, an emitter, and a collector;

a current source connected to the emitter of each of said first and second transistors;

a second pair of transistors including a third transistor and a fourth transistor, each of said third and fourth transistors having a base, an emitter, and a collector; and the emitter of each of said third and fourth transistors being connected to the collector of said first transistor; and

a third pair of transistors including a fifth transistor and a sixth transistor, each of said fifth and sixth transistors having a base, an emitter, and a collector; and the emitter of each of said fifth and sixth transistors being connected to the collector of said second transistor.

11. The cascaded latch chain in accordance with claim 9, wherein the two trans-admittance and trans-impedance stages in said at least one latch pair are clocked on opposite phases of a clock signal.

12. The cascaded latch chain in accordance with claim 7, further comprising a trans impedance stage latch connected to receive the output current of the last latch pair and produce an output voltage.

13. The cascaded latch chain in accordance with claim 8, further comprising a trans impedance stage latch connected to receive the output current of the last latch pair and produce an output voltage.

14. A latch pair comprising:

two independent combined trans-admittance and trans-impedance stages.

15. The latch pair in accordance with claim 14, wherein each trans-admittance stage comprises:

a first pair of transistors including a first transistor and a second transistor, the first and second transistors each having a base, an emitter, and a collector;

a current source connected to the emitter of each of said first and second transistors;

a second pair of transistors including a third transistor and a fourth transistor, each of said third and fourth transistors having a base, an emitter, and a collector; and the emitter of each of said third and fourth transistors being connected to the collector of said first transistor; and

a third pair of transistors including a fifth transistor and a sixth transistor, each of said fifth and sixth transistors having a base, an emitter, and a collector; and the emitter of each of said fifth and sixth transistors being connected to the collector of said second transistor.

16. The latch pair in accordance with claim 14, wherein the two trans-admittance and trans-impedance stages are clocked on opposite phases of a clock signal.